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1. (Amended) The media processing apparatus of Claim 72, wherein the data is received as a data stream including compressed AV data, wherein the media processing apparatus inputs the data stream, decodes data in the inputted data stream, and outputs the decoded AV data,

wherein said input/output processing means performs said input/output processes at a non-fixed rate, the input/output processes including inputting the data stream which is inputted at a non-fixed rate, storing data in the inputted data stream into a memory, and supplying the data stored in the memory to the decode processing means; and

the decode processing means which, in parallel with the input/output processing, performs the decode processing where decoding of the data stream stored in the memory is mainly performed, and

wherein the decoded AV data is stored in the memory, and

wherein the input/output processing means reads the decoded AV data from the memory, and respectively outputs the read AV data.

2. The media processing apparatus of Claim 1, wherein the decode processing means is composed of:

a sequential processing means for performing a sequential processing, which is mainly for condition judgements, on the data in the data stream, the sequential processing including a header analysis of the compressed audio data and the compressed video data and a decoding of the compressed audio data; and

a routine processing means for performing a routine processing in parallel with the sequential processing, the routine processing including a decoding of the compressed video date except for the header analysis.

3. The media processing apparatus of Claim 2,

wherein the sequential processing means alternates between performing a header analysis for analyzing a header which is assigned to a predetermined unit of data (hereinafter, called a "block") in the data stream and performing a decoding of the compressed audio data in the data stream, instructs the routine processing means to decode a block when the header analysis for the block is completed, and starts the header analysis of a next block when receiving notification from the routine processing means that the decoding of the block is completed; and

wherein the routine processing means decodes the compressed video data for a block in accordance with a result of the header analysis given by the sequential processing means.

4. The media processing apparatus of Claim 3, wherein the routine processing means is composed of:

a data translation means for performing variable length code decoding (abbreviated as the "VLD" hereafter) on the compressed video data of the data stream in accordance with an instruction from the sequential processing means;

a calculation means for performing inverse quantization (abbreviated as the "IQ" hereafter) and inverse discrete cosine transformation (abbreviated as the "IDCT" hereafter) by executing a predetermined calculation on a video block obtained through the VLD; and

a blending means for restoring video block data which corresponds to the video block by blending a decoded rectangular image of a frame stored in the memory with the video block data on which the IDCT has been performed.

5. The media processing apparatus of Claim 4, wherein the calculation means includes

a first buffer having a storage area whose capacity is equivalent to one block, and

wherein the data translation means includes:

a VLD means for performing the VLD on the compressed video data of the data stream;

a first address table means for storing a first address sequence where addresses in the first buffer are arranged in an order for a zigzag scan;

a second address table means for storing a second address sequence where addresses in the first buffer are arranged in an order for an alternate scan; and

a writing means for writing block data obtained through the VLD performed by the VLD means into the first buffer in accordance with one of the first address sequence and the second address sequence.

6. The media processing apparatus of Claim 5, wherein the writing means includes:

a table address generate means for sequentially generating a table address for the first address table means and the second address table means;

an address select means for sequentially selecting one of an address of the first address sequence and an address of the second address sequence which are separately outputted from the first table means and the second table means into which the table address has been inputted; and

an address output means for outputting the selected address to the first buffer.

7. The media processing apparatus of Claim 1, wherein the input/output processing means is composed of:

an input means for inputting an asynchronous data stream;

a video output means for outputting the decoded video data to the external display device;

an audio output means for outputting the decoded audio data to the external audio output device; and

a processor for executing task programs from a first task program to a fourth task program stored in an instruction memory, by switching between the four task programs, the task programs including:

the first task program for transferring the data stream from the input means to the memory;

the second task program for supplying the data stream from the memory to the decode processing means;

the third task program for outputting the decoded video data from the memory to the video output means; and

the fourth task program for outputting the decoded audio data from the memory to the audio output means.

8. The media processing apparatus of Claim 7, wherein the processor is composed of:

a program counter unit including at least four program counters corresponding to the task programs from the first task program to the fourth task program;

an instruction fetch unit for fetching an instruction from the instruction memory which stores the task programs, using an instruction address designated by one of the program counters;

an instruction execution unit for executing the instruction fetched by the instruction fetch unit; and

a task control unit for controlling the instruction fetch unit to sequentially switch the program counter every time a predetermined number of instruction cycles have elapsed.

9. The media processing apparatus of Claim 8, wherein the processor is further composed of

a register unit including at least four register sets corresponding to the program tasks from the first task program to the fourth task program, and

wherein the task control unit, simultaneously with switching of a program counter, switches a present register set to a register set which is to be used by the instruction execution unit.

10. The media processing apparatus of Claim 9, wherein the task control unit is composed of:

a counter for counting a number of instruction cycles in accordance with a clock signal every time the program counter is switched; and

a switch instruction unit for controlling the instruction fetch unit to switch the program counter when a count value of the counter reaches the predetermined number.

11. The media processing apparatus of Claim 10, wherein the decode processing means is composed of:

a sequential processing means for performing a sequential processing, which is mainly for condition judgements, on the data in the data stream, the sequential processing including a header analysis of the compressed audio data and the compressed video data and a decoding of the compressed audio data; and

a routine processing means for performing a routine processing in parallel with the sequential processing, the routine processing including a decoding of the compressed video data except for the header analysis.

12. The media processing apparatus of Claim 11, wherein the sequential processing means alternates between performing a header analysis for analyzing a header which is assigned to a predetermined unit of data (hereinafter, called a "block") in the data stream and performing a decoding of the compressed audio data in the data stream, instructs the routine processing means to decode a block when the header analysis for the block is completed, and starts the header analysis of a next block when receiving

notification from the routine processing means that the decoding of the block is completed; and

wherein the routine processing means decodes the compressed video data for a block in accordance with a result of the header analysis given by the sequential processing means.

13. The media processing apparatus of Claim 12,

wherein the routine processing means is composed of:

a data translation means for performing variable length code decoding (abbreviated as the "VLD" hereafter) on the compressed video data of the data stream in accordance with an instruction from the sequential processing means;

a calculation means for performing inverse quantization (abbreviated as the "IQ" hereafter) and inverse discrete cosine transformation (abbreviated as the "IDCT" hereafter) by executing a predetermined calculation on a video block obtained through the VLD; and

a blending means for restoring video block data which corresponds to the video block by blending a decoded rectangular image of a frame stored in the memory with the video block data on which the IDCT has been performed.

14. The media processing apparatus of Claim 13,

wherein the calculation means includes

a first buffer having a storage area whose capacity is

equivalent to one block, and

wherein the data translation means includes:

a VLD means for performing the VLD on the compressed video data of the data stream;

a first address table means for storing a first address sequence where addresses in the first buffer are arranged in an order for a zigzag scan;

a second address table means for storing a second address sequence where addresses in the first buffer are arranged in an order for an alternate scan; and

a writing means for writing block data obtained through the VLD performed by the VLD means into the first buffer in accordance with one of the first address sequence and the second address sequence.

15. The media processing apparatus of Claim 14,

wherein the writing means includes:

a table address generate means for sequentially generating a table address for the first address table means and the second address table means;

an address select means for sequentially selecting one of an address of the first address sequence and an address of the second address sequence which are separately outputted from the first table means and the second table means into which the table address has been inputted; and

an address output means for outputting the selected

16. (Amended) A media processing apparatus comprising:

an input means for inputting a data stream including compressed video data;

a sequential processing means for performing a sequential processing which is for condition judgements, the sequential processing including performing a header analysis for analyzing a header which is assigned to a predetermined unit of data (hereinafter, called a "block") in the data stream, wherein each block is a macroblock including a plurality of video blocks which each include luminance blocks and color-difference blocks; and

a routine processing means for performing, in parallel with the sequential processing, a routine processing which is mainly for routine calculations, the routine processing including a decoding of the compressed video data of the data stream for a block using a result of the header analysis, and

wherein the sequential processing means instructs the routine processing means to decode the block when the header analysis of the block is completed, and starts the header analysis of a next block when receiving notification from the routine processing means that the decoding of the block is completed.

17. The media processing apparatus of Claim 16,

wherein the routine processing means is composed of:

a data translation means for performing variable length code decoding (abbreviated as the "VLD" hereafter) on the compressed video data of the data stream in accordance with an instruction from the sequential processing means;

a calculation means for performing inverse quantization (abbreviated as the "IQ" hereafter) and inverse discrete cosine transformation (abbreviated as the "IDCT" hereafter) by executing a predetermined calculation on a video block obtained through the VLD; and

a blending means for restoring video block data by performing motion compensation processing which is achieved by blending the decoded block with the video block on which the IDCT has been performed, and

wherein the sequential processing means is composed of:

an obtaining means for obtaining header information on which the VLD has been performed by the data translation means;

an analyzing means for analyzing the obtained header information;

a notifying means for reporting parameters obtained as a result of the header analysis to the routine processing means;

an audio decoding means for decoding the compressed audio data of the data stream inputted by the input means; and

a control means for stopping an operation of the audio decoding means and activating the obtaining means when

receiving an interrupt signal from the routine processing means that indicates a decode completion of the block, and for instructing the data translation means to start the VLD on the compressed video data or the data stream when the parameters have been indicated by the notifying means.

18. The media processing apparatus of Claim 17,

wherein the analyzing means calculates a quantization scale and a motion vector in accordance with the header information, and

wherein the notifying means notifies the calculation means of the quantization scale and notifies the blending means of the motion vector.

19. The media processing apparatus of Claim 18, wherein the calculation means is composed of:

a first control storage unit and a second control storage unit which each store a microprogram;

a first program counter for designating a first read address to the first control storage unit;

a second program counter for designating a second read address;

a selector for selecting one of the first read address and the second read address and outputting the selected read address to the second control storage unit; and

an execution unit, which includes a multiplier and an

adder, for executing the IQ and IDCT in block units according to microprogram control by the first control storage unit and the second control storage unit.

20. The media processing apparatus of Claim 19, wherein the execution unit separately performs a processing using the multiplier and a processing using the adder in parallel when the second read address is selected by the selector, and performs the processing using the multiplier and the processing using the adder in coordination when the first read address is selected by the selector.

21. The media processing apparatus of Claim 20,

wherein the calculation means is further composed of:

a first buffer for holding a video block inputted from the data translation means; and

a second buffer for holding a video block on which the IDCT has been performed by the execution unit, and

wherein the first control storage unit stores a microprogram for the IQ and a microprogram for the IDCT,

wherein the second control storage unit stores a microprogram for the IDCT and a microprogram for transferring a video block on which the IDCT has been performed to the second buffer, and

wherein the execution means executes a processing to transfer the video block on which the IDCT has been performed

to the second buffer and the IQ processing of a next video block in parallel, and executes the IDCT processing of the next video block, on which the IQ processing has been performed, using the multiplier and the adder in coordination.

22. The media processing apparatus of Claim 21,

wherein the blending means further generates a differential block representing a differential image from video data which is to be compressed;

wherein the second buffer stores the generated differential block,

wherein the first control storage unit further stores a microprogram for discrete cosine transformation (abbreviated as the "DCT" hereafter) and a microprogram for quantization processing (abbreviated as the "Q processing" hereafter),

wherein the second control storage unit further stores a microprogram for the DCT and a microprogram for transferring the video block on which the DCT has been performed to the first buffer,

wherein the execution means further executes the DCT and Q processing on the differential block stored in the second buffer and transfers the differential block on which the DCT and Q processing has been performed to the first buffer,

wherein the data translation means further performs variable length coding (abbreviated as the "VLC" hereafter) on

the block stored in the first buffer, and

wherein the sequential processing means further assigns header information to a block on which the VLD has been performed by the data translation means.

23. The media processing apparatus of Claim 19,

wherein the input means further inputs polygon data,

wherein the sequential processing means further analyzes the polygon data and calculates vertex coordinates and edge inclinations of the polygon, and

wherein the routine processing means further generates image data of the polygon in accordance with the calculated vertex coordinates and edge inclinations.

24. The media processing apparatus of Claim 23,

wherein the first control storage unit and the second control storage unit each store a microprogram for performing a scan conversion based on a digital differential analyze algorithm, and

wherein the execution unit performs the scan conversion based on the vertex coordinates and edge inclinations calculated by the sequential processing means according to control of the microprogram.

25. The media processing apparatus of Claim 18, wherein the calculation means is composed of:

a first control storage unit and the second control storage unit for respectively storing a microprogram;

a first program counter for designating a first read address to the first control storage unit;

a second program counter for designating a second read address;

a selector for selecting one of the first read address and the second read address and outputting the selected address to the second control storage unit; and

a plurality of execution units for executing the IQ and IDCT in units of blocks according to control of the microprogram by the first control storage unit and the second control storage unit, each execution unit including a multiplier and an adder, and

wherein each execution unit takes charge of a partial block which is divided from the block.

26. The media processing apparatus of Claim 25, wherein the calculation means is further composed of:

a plurality of address translation tables which are set corresponding to the plurality of execution units, each address translation table storing translated addresses whose order is partially changed in a predetermined address sequence;

an instruction register group including a plurality of registers which each store a microinstruction associated with

one of the translated addresses, each microinstruction forming part of a microprogram that realizes a predetermined calculation; and

a switching unit, which is set between the first and second control storage units and the plurality of execution units, for outputting microinstructions from the instruction registers to the plurality of execution units in place of a microinstruction outputted from one of the first control storage unit and the selector to every execution unit, and

wherein when the first read address or the second read address is an address of the predetermined address sequence, the address is translated into the translated addresses by the address translation tables, and

wherein the instruction register group outputs the microinstructions corresponding to the translated addresses outputted from the address translation tables.

27. The media processing apparatus of Claim 26, wherein

when a microinstruction indicating one of an addition or subtraction operation is outputted from one of the instruction registers, each address translation table outputs a flag showing whether the microinstruction indicates an addition or a subtraction while the first program counter is outputting the first read address in the predetermined address sequence,

the plurality of execution units perform addition or subtraction in accordance with the flag, and

the flag is set in accordance with the microinstruction of the second control storage unit.

28. The media processing apparatus of Claim 26,

wherein the second control storage unit further outputs information showing a storage destination of a microinstruction execution result at a same time of an output of the microinstruction stored in the register while the first program counter outputs the first read address of the predetermined address sequence, and

wherein each execution unit stores the execution result in accordance with the storage destination information.

Claims 29-41 are cancelled

42. (Amended) A media processing apparatus which inputs a data stream including compressed audio/video (AV) data, decodes the inputted stream data, and outputs the decoded data, the media processing apparatus comprising:

an input/output processing means for performing input/output processes, the input/output processes including storing a data stream in a memory;

a sequential processing means for performing a sequential processing mainly for condition judgements, the sequential processing including a header analysis of compressed video data in the compressed AV data and a decoding of compressed audio data in the compressed AV data, whereby the decoded audio data is stored in the memory; and

a routine processing means for performing a routine processing mainly for routine calculations on the compressed video data stored in the memory in accordance with a result of the header analysis given by the sequential processing means, the routine processing including a decoding of the compressed video data, whereby the decoded video data is stored in the memory, and

wherein the input/output processing further includes reading the decoded audio data and the decoded video data from the memory and respectively outputting the read audio data and the read video data,

wherein the header analysis is a header analysis of a macroblock including a plurality of video blocks.

43. The media processing apparatus of Claim 42,

wherein the sequential processing means alternates between performing a header analysis for analyzing a header which is assigned to a predetermined unit of data (hereinafter, called a "block") in the data stream and performing a decoding of the compressed audio data in the data stream, instructs the routine processing means to decode a block when the header analysis for the block is completed, and starts the header analysis of a next block when receiving notification from the routine processing means that the decoding of the block is completed; and

wherein the routine processing means decodes the compressed video data for a block in accordance with a result of the header analysis given by the sequential processing means.

44. The media processing apparatus of Claim 43,

wherein the routine processing means is composed of:

a data translation means for performing variable length code decoding (abbreviated as the "VLD" hereafter) on the compressed video data of the data stream in accordance with an instruction from the sequential processing means;

a calculation means for performing inverse quantization (abbreviated as the "IQ" hereafter) and inverse discrete cosine transformation (abbreviated as the "IDCT" hereafter) by executing a predetermined calculation on a video block

obtained through the VLD; and

a blending means for restoring video block data which corresponds to the video block by blending a decoded rectangular image of a frame stored in the memory with the video block data on which the IDCT has been performed.

45. The media processing apparatus of Claim 44, wherein the calculation means includes

a first buffer having a storage area whose capacity is equivalent to one block, and

wherein the data translation means includes:

a VLD means for performing the VLD on the compressed video data of the data stream;

a first address table means for storing a first address sequence where addresses in the first buffer are arranged in an order for a zigzag scan;

a second address table means for storing a second address sequence where addresses in the first buffer are arranged in an order for an alternate scan; and

a writing means for writing block data obtained through the VLD performed by the VLD means into the first buffer in accordance with one of the first address sequence and the second address sequence.

46. The media processing apparatus of Claim 45, wherein the writing means includes:

a table address generate means for sequentially generating a table address for the first address table means and the second address table means;

an address select means for sequentially selecting one of an address of the first address sequence and an address of the second address sequence which are separately outputted from the first table means and the second table means into which the table address has been inputted; and

an address output means for outputting the selected address to the first buffer.

47. The media processing apparatus of Claim 42,

wherein the input/output processing means is composed of:

an input means for inputting an asynchronous data stream;

a video output means for outputting the decoded video data to the external display device;

an audio output means for outputting the decoded audio data to the external audio output device; and

a processor for executing task programs from a first task program to a fourth task program stored in an instruction memory, by switching between the four task programs, the task programs including:

the first task program for transferring the data stream from the input means to the memory;

the second task program for supplying the data stream from the memory to the decode processing means;

the third task program for outputting the decoded video data from the memory to the video output means; and

the fourth task program for outputting the decoded audio data from the memory to the audio output means.

48. The media processing apparatus of Claim 47, wherein the processor is composed of:

a program counter unit including at least four program counters corresponding to the task programs from the first task program to the fourth task program;

an instruction fetch unit for fetching an instruction from the instruction memory which stores the task programs, using an instruction address designated by one of the program counters;

an instruction execution unit for executing the instruction fetched by the instruction fetch unit; and

a task control unit for controlling the instruction fetch unit to sequentially switch the program counter every time a predetermined number of instruction cycles have elapsed.

49. The media processing apparatus of Claim 48, wherein the processor is further composed of

a register unit including at least four register sets

corresponding to the program tasks from the first task program to the fourth task program, and

wherein the task control unit, simultaneously with switching of a program counter, switches a present register set to a register set which is to be used by the instruction execution unit.

50. The media processing apparatus of Claim 49, wherein the task control unit is composed of:

a counter for counting a number of instruction cycles in accordance with a clock signal every time the program counter is switched; and

a switch instruction unit for controlling the instruction fetch unit to switch the program counter when a count value of the counter reaches the predetermined number.

51. The media processing apparatus of Claim 49, wherein the routine processing means is composed of:

a data translation means for performing variable length code decoding (abbreviated as the "VLD" hereafter) on the compressed video data of the data stream in accordance with an instruction from the sequential processing means;

a calculation means for performing inverse quantization (abbreviated as the "IQ" hereafter) and inverse discrete cosine transformation (abbreviated as the "IDCT" hereafter) by executing a predetermined calculation on a video block.

obtained through the VLD; and

a blending means for restoring video block data which corresponds to the video block by blending a decoded rectangular image of a frame stored in the memory with the video block data on which the IDCT has been performed.

52. The media processing apparatus of Claim 51,

wherein the analyzing means calculates a quantization scale and a motion vector in accordance with the header information, and

wherein the notifying means notifies the calculation means of the quantization scale and notifies the blending means of the motion vector.

53. The media processing apparatus of Claim 52,

wherein the calculation means is composed of:

a first control storage unit and a second control storage unit which each store a microprogram;

a first program counter for designating a first read address to the first control storage unit;

a second program counter for designating a second read address;

a selector for selecting one of the first read address and the second read address and outputting the selected read address to the second control storage unit; and

an execution unit, which includes a multiplier and an

adder, for executing the IQ and IDCT in block units according to microprogram control by the first control storage unit and the second control storage unit.

54. The media processing apparatus of Claim 53,

wherein the execution unit separately performs a processing using the multiplier and a processing using the adder in parallel when the second read address is selected by the selector, and performs the processing using the multiplier and the processing using the adder in coordination when the first read address is selected by the selector.

55. The media processing apparatus of Claim 54,

wherein the calculation means is further composed of:

a first buffer for holding a video block inputted from the data translation means; and

a second buffer for holding a video block on which the IDCT has been performed by the execution unit, and

wherein the first control storage unit stores a microprogram for the IQ and a microprogram for the IDCT,

wherein the second control storage unit stores a microprogram for the IDCT and a microprogram for transferring a video block on which the IDCT has been performed to the second buffer, and

wherein the execution means executes a processing to transfer the video block on which the IDCT has been performed

to the second buffer and the IQ processing of a next video block in parallel, and executes the IDCT processing of the next video block, on which the IQ processing has been performed, using the multiplier and the adder in coordination.

56. The media processing apparatus of Claim 55,

wherein the blending means further generates a differential block representing a differential image from video data which is to be compressed;

wherein the second buffer stores the generated differential block,

wherein the first control storage unit further stores a microprogram for discrete cosine transformation (abbreviated as the "DCT" hereafter) and a microprogram for quantization processing (abbreviated as the "Q processing" hereafter),

wherein the second control storage unit further stores a microprogram for the DCT and a microprogram for transferring the video block on which the DCT has been performed to the first buffer,

wherein the execution means further executes the DCT and Q processing on the differential block stored in the second buffer and transfers the differential block on which the DCT and Q processing has been performed to the first buffer,

wherein the data translation means further performs variable length coding (abbreviated as the "VLC" hereafter) on

the block stored in the first buffer, and

wherein the sequential processing means further assigns header information to a block on which the VLD has been performed by the data translation means.

57. The media processing apparatus of Claim 52,

wherein the calculation means is composed of:

a first control storage unit and the second control storage unit for respectively storing a microprogram;

a first program counter for designating a first read address to the first control storage unit;

a second program counter for designating a second read address;

a selector for selecting one of the first read address and the second read address and outputting the selected address to the second control storage unit; and

a plurality of execution units for executing the IQ and IDCT in units of blocks according to control of the microprogram by the first control storage unit and the second control storage unit, each execution unit including a multiplier and an adder, and

wherein each execution unit takes charge of a partial block which is divided from the block.

58. The media processing apparatus of Claim 57,

wherein the calculation means is further composed of:

a plurality of address translation tables which are set corresponding to the plurality of execution units, each address translation table storing translated addresses whose order is partially changed in a predetermined address sequence;

an instruction register group including a plurality of registers which each store a microinstruction associated with one of the translated addresses, each microinstruction forming part of a microprogram that realizes a predetermined calculation; and

a switching unit, which is set between the first and second control storage units and the plurality of execution units, for outputting microinstructions from the instruction registers to the plurality of execution units in place of a microinstruction outputted from one of the first control storage unit and the selector to every execution unit, and

wherein when the first read address or the second read address is an address of the predetermined address sequence, the address is translated into the translated addresses by the address translation tables, and

wherein the instruction register group outputs the microinstructions corresponding to the translated addresses outputted from the address translation tables.

59. The media processing apparatus of Claim 58, wherein

when a microinstruction indicating one of an addition or subtraction operation is outputted from one of the instruction registers, each address translation table outputs a flag showing whether the microinstruction indicates an addition or a subtraction while the first program counter is outputting the first read address in the predetermined address sequence,

the plurality of execution units perform addition or subtraction in accordance with the flag, and

the flag is set in accordance with the microinstruction of the second control storage unit.

60. The media processing apparatus of Claim 58,

wherein the second control storage unit further outputs information showing a storage destination of a microinstruction execution result at a same time of an output of the microinstruction stored in the register while the first program counter outputs the first read address of the predetermined address sequence, and

wherein each execution unit stores the execution result in accordance with the storage destination information.

61. The media processing apparatus of Claim 51,

wherein the calculation means includes

a first buffer having a storage area whose capacity is equivalent to one block, and

wherein the data translation means includes:

a VLD means for performing the VLD on the compressed video data of the data stream;

a first address table means for storing a first address sequence where addresses in the first buffer are arranged in an order for a zigzag scan;

a second address table means for storing a second address sequence where addresses in the first buffer are arranged in an order for an alternate scan; and

a writing means for writing block data obtained through the VLD performed by the VLD means into the first buffer in accordance with one of the first address sequence and the second address sequence.

62. The media processing apparatus of Claim 61, wherein the writing means includes:

a table address generate means for sequentially generating a table address for the first address table means and the second address table means;

an address select means for sequentially selecting one of an address of the first address sequence and an address of the second address sequence which are separately outputted from the first table means and the second table means into which the table address has been inputted; and

an address output means for outputting the selected address to the first buffer.

63. The media processing apparatus of Claim 62,

wherein the analyzing means calculates a quantization scale and a motion vector in accordance with the header information, and

wherein the notifying means notifies the calculation means of the quantization scale and notifies the blending means of the motion vector.

64. The media processing apparatus of Claim 63, wherein the calculation means is composed of:

a first control storage unit and a second control storage unit which each store a microprogram;

a first program counter for designating a first read address to the first control storage unit;

a second program counter for designating a second read address;

a selector for selecting one of the first read address and the second read address and outputting the selected read address to the second control storage unit; and

an execution unit, which includes a multiplier and an adder, for executing the IQ and IDCT in block units according to microprogram control by the first control storage unit and the second control storage unit.

65. The media processing apparatus of Claim 64, wherein the execution unit separately performs a

processing using the multiplier and a processing using the adder in parallel when the second read address is selected by the selector, and performs the processing using the multiplier and the processing using the adder in coordination when the first read address is selected by the selector.

66. The media processing apparatus of Claim 65, wherein the calculation means is further composed of a second buffer for holding a video block on which the IDCT has been performed by the execution unit, and

wherein the first control storage unit stores a microprogram for the IQ and a microprogram for the IDCT,

wherein the second control storage unit stores a microprogram for the IDCT and a microprogram for transferring a video block on which the IDCT has been performed to the second buffer, and

wherein the execution means executes a processing to transfer the video block on which the IDCT has been performed to the second buffer and the IQ processing of a next video block in parallel, and executes the IDCT processing of the next video block, on which the IQ processing has been performed, using the multiplier and the adder in coordination.

67. The media processing apparatus of Claim 66, wherein the blending means further generates a differential block representing a differential image from

video data which is to be compressed;

wherein the second buffer stores the generated differential block,

wherein the first control storage unit further stores a microprogram for discrete cosine transformation (abbreviated as the "DCT" hereafter) and a microprogram for quantization processing (abbreviated as the "Q processing" hereafter),

wherein the second control storage unit further stores a microprogram for the DCT and a microprogram for transferring the video block on which the DCT has been performed to the first buffer,

wherein the execution means further executes the DCT and Q processing on the differential block stored in the second buffer and transfers the differential block on which the DCT and Q processing has been performed to the first buffer,

wherein the data translation means further performs variable length coding (abbreviated as the "VLC" hereafter) on the block stored in the first buffer, and

wherein the sequential processing means further assigns header information to a block on which the VLD has been performed by the data translation means.

68. The media processing apparatus of Claim 63, wherein the calculation means is composed of:

a first control storage unit and the second control

storage unit for respectively storing a microprogram;

a first program counter for designating a first read address to the first control storage unit;

a second program counter for designating a second read address;

a selector for selecting one of the first read address and the second read address and outputting the selected address to the second control storage unit; and

a plurality of execution units for executing the IQ and IDCT in units of blocks according to control of the microprogram by the first control storage unit and the second control storage unit, each execution unit including a multiplier and an adder, and

wherein each execution unit takes charge of a partial block which is divided from the block.

69. The media processing apparatus of Claim 68,

wherein the calculation means is further composed of:

a plurality of address translation tables which are set corresponding to the plurality of execution units, each address translation table storing translated addresses whose order is partially changed in a predetermined address sequence;

an instruction register group including a plurality of registers which each store a microinstruction associated with one of the translated addresses, each microinstruction forming

part of a microprogram that realizes a predetermined calculation; and

a switching unit, which is set between the first and second control storage units and the plurality of execution units, for outputting microinstructions from the instruction registers to the plurality of execution units in place of a microinstruction outputted from one of the first control storage unit and the selector to every execution unit, and

wherein when the first read address or the second read address is an address of the predetermined address sequence, the address is translated into the translated addresses by the address translation tables, and

wherein the instruction register group outputs the microinstructions corresponding to the translated addresses outputted from the address translation tables.

70. The media processing apparatus of Claim 69, wherein

when a microinstruction indicating one of an addition or subtraction operation is outputted from one of the instruction registers, each address translation table outputs a flag showing whether the microinstruction indicates an addition or a subtraction while the first program counter is outputting the first read address in the predetermined address sequence,

the plurality of execution units perform addition or

subtraction in accordance with the flag, and

the flag is set in accordance with the microinstruction of the second control storage unit.

71. The media processing apparatus of Claim 69,

wherein the second control storage unit further outputs information showing a storage destination of a microinstruction execution result at a same time of an output of the microinstruction stored in the register while the first program counter outputs the first read address of the predetermined address sequence, and

wherein each execution unit stores the execution result in accordance with the storage destination information.

72. (Amended) A media processing apparatus for decompressing compressed video data inputted from an outside source, comprising:

a processor for performing input/output processing affected by external factors, wherein said input/output processing includes at least inputting said compressed video data from outside and outputting decompressed video data to an external device; and

a video decoding means for decompressing said compressed video data supplied by said processor, wherein said processor processes in parallel with said video decoding means.

73. (New) The media processing apparatus of Claim 72,

wherein the processor includes

an instruction memory for storing a plurality of task programs that show contents of the input/output processing,

wherein the processor switches between and executes the plurality of task programs.

74. (New) The media processing apparatus of Claim 73,

wherein the processor further includes:

a program counter unit having a plurality of program counters that correspond to the plurality of task programs, respectively;

an instruction fetch unit that fetches instructions one by one from the instruction memory in accordance with instruction addresses indicated by one of the plurality of program counters;

an instruction execution unit that executes the fetched instructions one by one; and

a task control unit that switches from a currently executed task program to another by instructing the instruction fetch unit to fetch instructions in accordance with instruction addresses indicated by another program counter.

75. (New) The media processing apparatus of Claim 74,

wherein the task control unit switches from the currently executed task program to another when a predetermined number of instruction cycles, which is determined differently for each task program, passes, one instruction cycle corresponding to fetching and execution of one instruction.